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Inventor(s): **Hayden C. CRANFORD, Jr.** and **Joseph M. STEVENS**

METHOD AND CIRCUIT FOR INCREASED NOISE IMMUNITY FOR CLOCKING SIGNALS IN HIGH SPEED DIGITAL SYSTEMS

FIELD OF THE INVENTION

The present invention relates to clock signal buffering with high noise immunity for high speed digital systems.

BACKGROUND OF THE INVENTION

Clock signals within integrated circuits are utilized to control the movement of data and synchronize control signals. Typically, a specified amount of time after the estimated receipt of the leading edge of a clock signal, data transfer is accomplished within the integrated circuit. Many prior art methods for clock distribution are plagued by distortions or delays on the rising edge of the clock signal. If the rising edge is too late, the data transfer does not occur as required.

Large designs require many different circuits to be synchronized and operate at the same speed. In such systems, a high frequency clock signal must be distributed over a large chip area. Currently, attempts to distribute clock signals in the range of one gigahertz are

faltering due to the parasitic properties of long wires and long wire terminations. As the attenuation of the transmission line circuit and wiring load increases, the clock signal power level at transmission line terminations (circuit clock inputs) decreases. Transmission line circuit loading and interconnect wiring attenuation can be very high in present systems. A sub-circuit receiving a weak clock signal can cause serious design difficulties.

The propagation delay of a signal, due to long wires and multiple sinks, can be reduced by "repowering" or relaying the signal utilizing simple amplifiers, called buffers. Figure 1 illustrates a current solution in buffering clock signals in digital communications systems. The approach is to buffer a single clock signal from a clock source 10 referenced to a common ground and a common power supply with a "single-ended" buffer circuit 12a for a load circuit 14a. As more circuits 14b...14n are added to a given clock source, more "single-ended" buffer circuits 12b...12n are added in series to buffer the clocking signal from the source 10 to the destination circuit 14. Unfortunately, more noise is added to the clocking signal as each additional circuit is added to the clock signal path. Further, buffers introduce uncertainties in the timing of integrated circuits and require chip area.

Accordingly, a need exists for an integrated circuit clock distribution system that has high noise immunity and readily accommodates additional circuits in a clock signal path. The present invention addresses such a need.

SUMMARY OF THE INVENTION

Aspects for increased noise immunity for clocking signals in high speed digital systems are described. The aspects include buffering a differential clock signal with a single

buffer circuit for a plurality of load circuits and configuring the single buffer circuit to adjust to alterations in the number of load circuits receiving the differential clock signal. The configuring achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits.

With the present invention, a differential clock signal is utilized with the two output clock signals referenced to each other for small-swing signaling. Small-swing signaling keeps voltage amplitude well below half of the supply voltages, while better noise rejection results from the referencing of the differential signals to each other. High noise immunity is also enhanced from the use of a single buffer circuit, thus avoiding multiple stages of serial buffering. In addition, the present invention is configurable and allows for additional circuits to be added onto the clock signal source. Thus, a straightforward and effective manner of achieving an integrated circuit clock distribution system with high noise immunity is achieved. These and other advantages of the aspects of the present invention will be more fully understood in conjunction with the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a block diagram of a solution in buffering clock signals in digital communications systems in accordance with the prior art.

Figure 2 illustrates a block diagram of a solution in buffering clock signals in digital communications systems in accordance with the present invention.

Figure 3 illustrates a circuit diagram of a preferred embodiment of the differential amplifier with the programmable output impedance and programmable current source for the single buffer circuit of Figure 2.

DETAILED DESCRIPTION

The present invention relates to clock signal buffering with increased nose immunity in high speed digital systems. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

Referring now to Figure 2, clock buffering in accordance with the present invention utilizes a single clock source 20, and a single buffer circuit 22, where the single buffer circuit 22 is configurable and controlled via an impedance/current control circuit 24 for N number of load circuits 26a, 26b, ... 26n. A differential clock signal references true and complement clock signals (INT and INC) to each other for small-swing signaling. The single buffer circuit 22 includes a differential amplifier that has a programmable output impedance and a programmable current source controlled by control signals of the impedance/current control circuit, as described more particularly hereinbelow with reference to Figure 3. In general, for a particular capacitive load (CL), the output impedance (ZO) is

adjusted to the frequency bandwidth (FBW) needed on the clocking signal, where FBW = (CL)(ZO) (i.e., the output impedance is inversely proportional to the capacitive loading). Further, the output levels are proportional to output impedance and current drive (I) according to Vswing = (ZO)(I), so that the output impedance is inversely proportional to the current also.

Figure 3 illustrates a circuit diagram of a preferred embodiment of the differential amplifier with the programmable output impedance and programmable current source for the single buffer circuit 22 of the present invention. True and complement input signals of the differential clock signal (INT and INC) are received in each half of the differential amplifier portion of the circuit (designated by the dashed boxes) via steering devices 30 (e.g., transistors) M1 and M2 and output from the circuit (OUTA and OUTB) as indicated and as well understood in the art. Within each half of the differential amplifier, a first resistor 32 (R1) is coupled to a power supply and coupled in parallel to N additional resistors 34 of known value (RT1...RTn for the true half and RC1...RCn for the complement half) via corresponding switches 36. The additional resistors 34 are selectively added to the circuit via control signals (CT1...CTn), such as from a controller (not shown), that activate their respective switches 36 (MT1...MTn and MC1...MCn). In the embodiment shown, the switches 36 are active low and activated by a low level control signal. Further included in the circuit is a current source device 40. The current source device 40 is coupled in parallel to N additional current source devices 42, where each additional current source device 42 is switched in when selected via activation of the respective switch 44 by the corresponding

control signal (CT1...CTn). The current source devices 40, 42 and switches 44 are standard components biased by a BIAS voltage, as is well understood in the art.

With this circuitry, the overall output impedance and current drive level can be adjusted in tandem in inverse proportion by the activation of the control signals to switch resistors and current source devices in and out as necessary. For example, activation of control signal CT1, activates switches MT1/MC1 and MS1, so that resistance RT1/RC1 is added in to reduce the overall impedance and current source MCS1 is added in to increase the current drive level. Thus, the result of a programmable output impedance in the differential amplifier is a constant bandwidth as more load is added. The result of the programmable current source and output impedance being adjusted together is a constant output voltage from the differential amplifier circuit. In this manner, the number of circuits receiving the clock signal source can be increased as desired without increasing the noise, since the present invention lacks multiple stages of serial buffering.

Although the present invention has been described in accordance with the embodiments shown, one of ordinary skill in the art will readily recognize that there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the appended claims.